

REMARKS

Claims 52-53 and 56 have been amended. No claims have been canceled. No new claims have been added. Claims 37-61 are pending.

Claims 53 and 56 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 52 has been amended to recite "a first field effect transistor" and "a first bipolar transistor." Claim 53 has been amended to recite that the first load circuit "further comprises a second field effect transistor." Claim 56 has been amended to recite that the second load circuit "further comprises a second bipolar transistor." Accordingly, the rejection under 35 U.S.C. § 112, second paragraph to claims 53 and 56 should be withdrawn.

Claims 37-42 and 46-51 stand rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claim 9 of U.S. Patent No. 6,738,297. Claims 43-45 and 59-61 stand rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claim 25 of U.S. Patent No. 6,738,297. Claims 52-58 stand rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claim 9-15 of U.S. Patent No. 6,738,297.

A Terminal Disclaimer with respect to U.S. Patent No. 6,738,297 is being concurrently filed with this amendment. Accordingly, the double patenting rejections to claims 37-61 should be withdrawn.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Dated: December 15, 2004

Respectfully submitted,

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